



D5062
MS-S3681

Server Motherboard
User Guide

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V1.1, 2026/07

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Safety Information



Please read and follow these safety instructions carefully before installing, operating or performing maintenance on the server.

General Safety Instructions

- Always read the safety instructions carefully.
- Keep this User Guide for future reference.
- Keep this equipment away from humidity.
- Lay the equipment on a stable, flat surface before setting it up.
- Do not cover the air openings to prevent overheating.
- Avoid spilling liquids into the equipment to prevent damage or electrical shock.
- Do not leave the equipment in an unconditioned environment. Storage temperatures above 60°C (140°F) may cause damage.

Electrical Safety

Power Setup and Protection

- Ensure the power source matches the equipment voltage before connection.
- Plug the power cord into a grounded (earthed) electrical outlet that is easily accessible at all times. Do not disable the power cord grounding plug, as it is an important safety feature.
- Do not use a power adapter other than the one provided.
- Place the power cord to avoid being stepped on or crushed.
- Protect the server from power fluctuations and outages using a regulated uninterruptible power supply (UPS).

Handling Power Connections

- Unplug the power cord before inserting add-on cards or modules.
- Disconnect all power supplies before maintenance to avoid electrical shock. If the unit has more than one power supply, disconnect all of them.
- Unplug the power cord to fully disconnect the system. The front panel Power On/Standby button does not completely shut off system power. Portions of the power supply and some internal circuitry remain active until AC/DC power is removed.

Assembly and Installation

This equipment must be installed in restricted access areas by qualified personnel to comply with safety standards set by the NEC and IEC 62368-1, Third Edition, for Information Technology Equipment.

Lifting and Placement

WARNING: This server is heavy.

- Follow occupational health and safety guidelines for manual material handling.
- A minimum of two people is required to lift or install the server. For installations above chest height, a third person may be needed for alignment.
- Exercise caution when installing or removing the server from the rack, as it may become unstable when not fastened to the rails.

Hot Surfaces

- Allow components like drives and power supplies to cool before touching.

Energy Pack Handling after Removal

To reduce the risk of fire or burns:

- Do not disassemble, crush, or puncture the energy pack.
- Avoid shorting external contacts.
- Do not dispose of the energy pack in fire or water.

Other Components

- Keep away from hazardous moving parts, such as fan blades, to prevent injury.
- Do not drop or jolt the system, as this may damage internal components or compromise safety.

General Precautions During Operation

- Avoid operating the server with the access panel open or removed for extended periods, as this disrupts airflow and may cause overheating.
- Do not insert incorrect connectors into ports to avoid damage to components or the risk of electrical hazards.
- This equipment is not suitable for use in locations where children are likely to be present.

When to Contact Service Personnel

Seek immediate assistance from qualified personnel if any of the following occurs:

- The power cord or plug is damaged.
- Liquid has entered the equipment.
- The equipment has been exposed to moisture.
- The equipment does not function as described in the User Guide.
- The equipment has been dropped or physically damaged.
- The equipment shows visible signs of breakage.

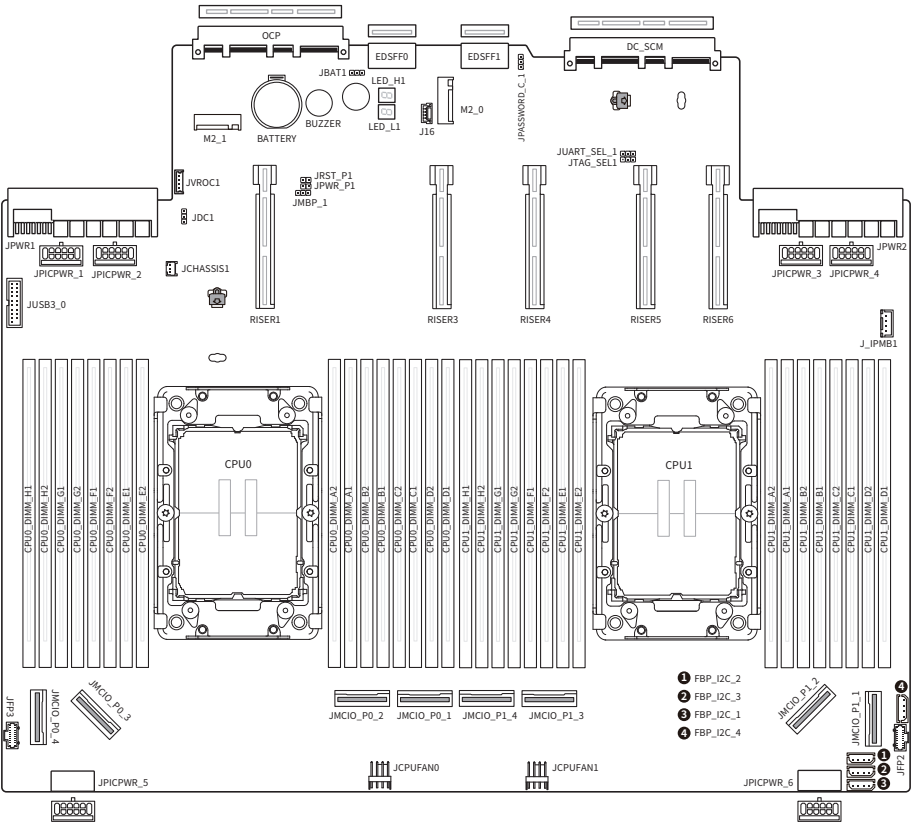
Specifications

Model	D5052
Form factor	DC-MHS M-FLW
Dimensions	423mm x 348mm
Processor	Dual Intel® Xeon® 6700E-series, 6500P-series and 6700P-series processors, TDP up to 350W
Socket	2 x Intel® LGA 4710 (Socket E2)
Memory	<ul style="list-style-type: none"> • 32 x DDR5 DIMM slots, 8 channels per CPU (2DPC), RDIMM/ MRDIMM* <ul style="list-style-type: none"> - Max Frequency: <ul style="list-style-type: none"> » RDIMM: 6500P/ 6700P series: 6400 MT/s (1DPC), 6000 MT/s (2DPC) 6700E series: 6400 MT/s (1DPC), 5200 MT/s (2DPC) » MRDIMM*: 8000 MT/s (only support 1DPC) - Max Capacity per DIMM: <ul style="list-style-type: none"> » RDIMM: 256GB » MRDIMM: 64GB <p>*MRDIMMs are only supported with Intel® Xeon® 6 P-core series processors.</p>
Storage	<ul style="list-style-type: none"> • 2 x 2280/22110 PCIe 5.0 x2 NVMe M.2 slots (from CPU0) • 2 x E1.S 9.5mm PCIe 5.0 x4 ports (from CPU1)
Expansions	<ul style="list-style-type: none"> • 5 x PCIe 5.0 x16 SFF-TA-1033 MXIO slots(2 from CPU0, 3 from CPU1) • 8 x Far-side PCIe 5.0 x8 MCIO 8i connectors (4 from CPU0, 4 from CPU1)
Networking	1 x PCIe 5.0 x16 OCP 3.0 slot (from CPU0, NCSI supported)
RAID	NVMe RAID 0/1/5/10 (Intel® VROC RAID key required)
Graphics	Supports via DC-SCM module MGT1
Audio	N/A
USB	1 x 20-pin USB 3.2 Gen 1 header (5 Gbps, internal, for 2 USB ports)
Rear I/O	Supports via DC-SCM module MGT1
System Connectors	<ul style="list-style-type: none"> • 1 x Edge slot for DC-SCM 2.0 module (MGT1) • 2 x DC-MHS control panel header for front panel (1 left, 1 right) • 2 x 4-pin fan connectors (for debug) • 1 x 4-pin liquid leak detection connector • 1 x Power button header • 1 x Reset button header • 1 x IPMB header • 1 x VROC connector • 4 x I2C headers • 1 x Chassis intrusion header • 1 x Buzzer

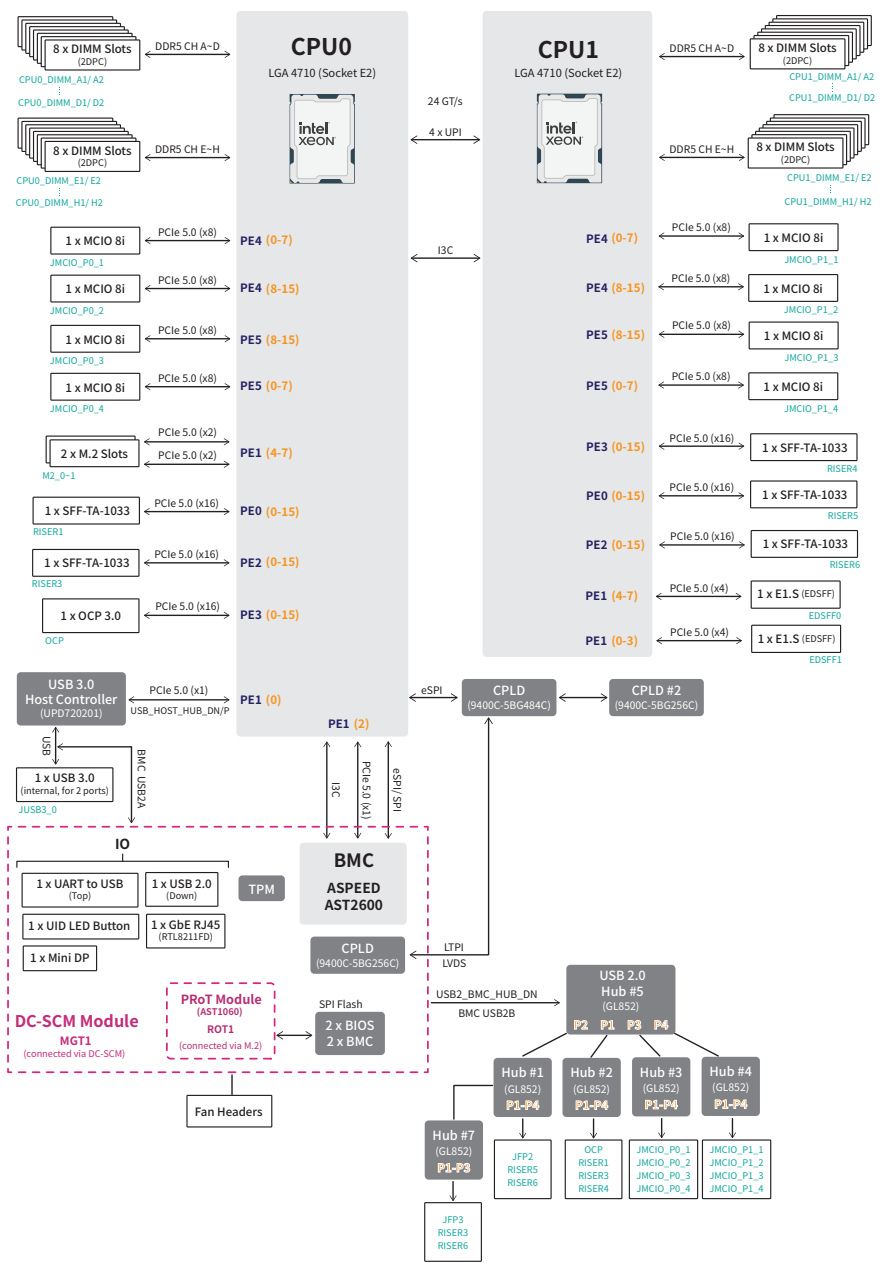
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Model	D5052
Power Connectors	<ul style="list-style-type: none"> • 2 x CRPS/M-CRPS 185 x 73.5mm power connectors • 6 x 12-pin PICPWR power connectors
Security	<ul style="list-style-type: none"> • Chassis intrusion (on board header) • Supports via DC-SCM module MGT1: <ul style="list-style-type: none"> - TPM 2.0 module (optional) - ASPEED AST1060 Hardware Root-of-Trust module (optional)
Server Management	<ul style="list-style-type: none"> • Supports via DC-SCM module MGT1: <ul style="list-style-type: none"> - 1 x 1000Base-T dedicated server management port <ul style="list-style-type: none"> » ASPEED AST2600 with AMI MegaRAC based firmware » Supports IPMI 2.0 and DMTF Redfish® API • Dual BIOS and dual BMC, with eMMC for local BMC storage media
Environment	<ul style="list-style-type: none"> • Operating Temperature: 10°C ~ 35°C (50°F ~ 95°F) • Operating Humidity: 8% to 85% (non-condensing) • Non-operating Temperature: -30°C ~ 60°C (-40°F to 140°F) • Non-operating Relative Humidity: 8% to 90% (non-condensing)
Certifications	CE, FCC (Class A)

Overview of Components



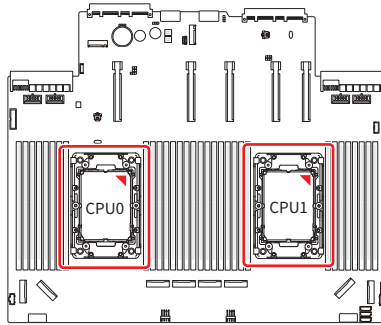
Block Diagram



Component Contents

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LED_H1, LED_L1: Port 80 Debug LEDs	43

CPU Socket



Important

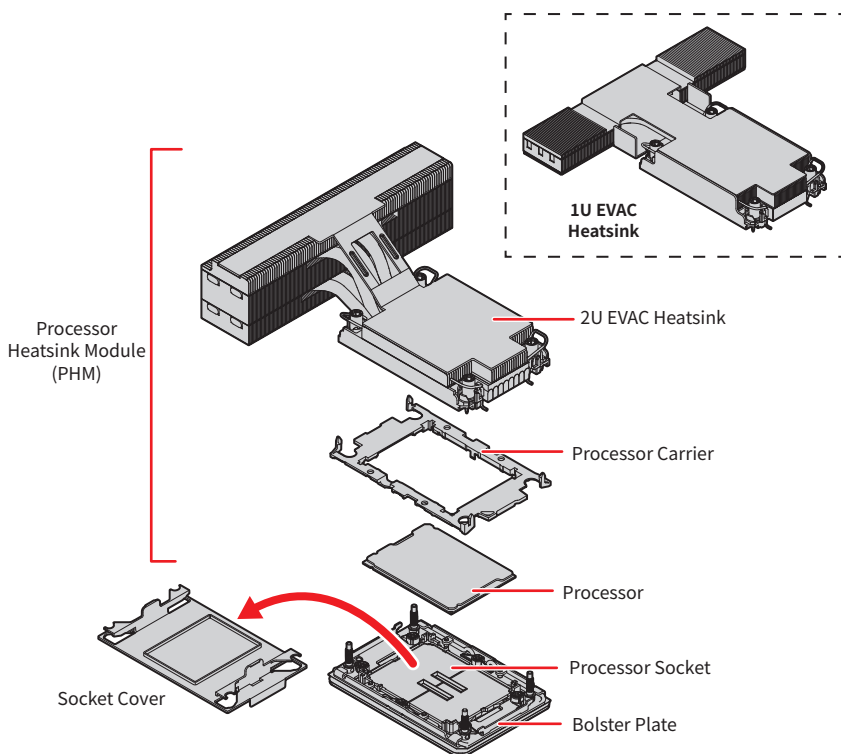
- **Overheating** will seriously damage the CPU and system. Always make sure the cooling fan can work properly to protect the CPU from overheating. Make sure that you apply an even layer of thermal paste (or thermal tape) between the CPU and the heatsink to enhance heat dissipation.
- While **replacing the CPU**, always turn off the power supply or unplug the power supply's power cord from the grounded outlet first to ensure the safety of CPU.

Assembly Overview



Important

Illustrations are for demonstration purposes only; actual parts may vary.

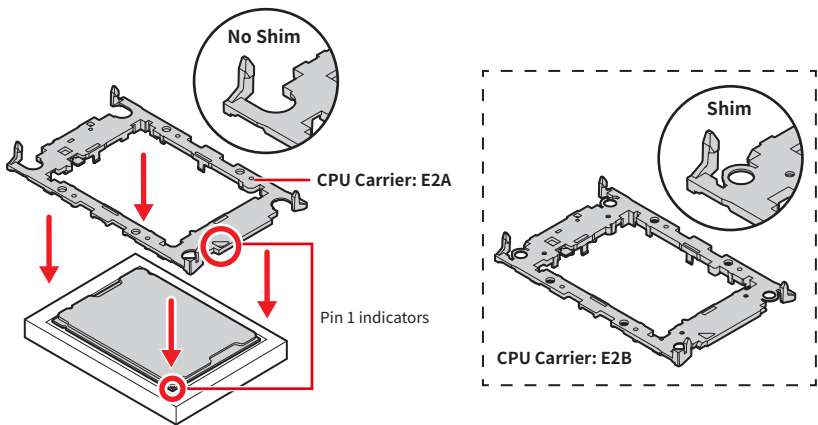


Important

- Please check the instruction that come with your heatsink and thermal paste for more details before starting.
- Confirm if your heatsink is firmly installed before turning on your system.
- Whenever CPU is not installed, always protect your CPU socket pins with the plastic cap covered.
- Do not touch the CPU socket content to avoid damage.
- Read the CPU status in BIOS.

Installing CPU & Heatsink

- 1. Place the processor carrier on top of the processor in the tray with their **pin 1 indicators aligned**. If installed properly, the CPU will snap into the carrier's side latches and the carrier will latch firmly to it.

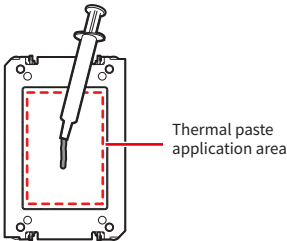


Important

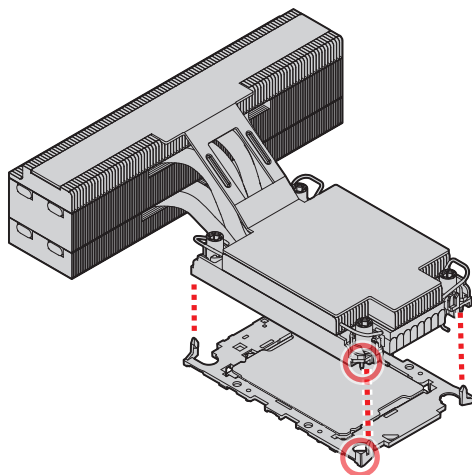
- Do not touch the CPU package land to avoid damage.
- Please refer to the following table for the corresponding CPU carrier.

CPU Package Type	Thin Package	Thick Package
CPU Package Name	• Granite Rapids- SP XCC	• Granite Rapids- SP HCC/ LCC • Sierra Forest- SP
CPU Carrier Code	E2A	E2B
Shim	No	Yes
Integrated TIM Break Lever	Yes	Yes

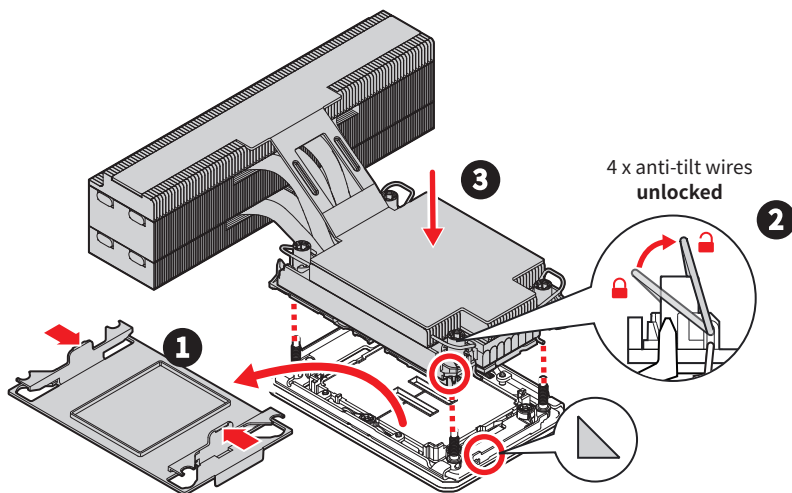
- 2. Remove the **protective film** at the bottom of the heatsink if any.
- To avoid damaging the fins of the heatsink, always grip the heatsink **along the axis of the fins**. Holding a heatsink along the side might damage its fins or solder.
- 3. Make sure the heatsink has **pre-applied thermal paste**. If there isn't, you'll need to apply thermal paste to the bottom center of the heatsink.



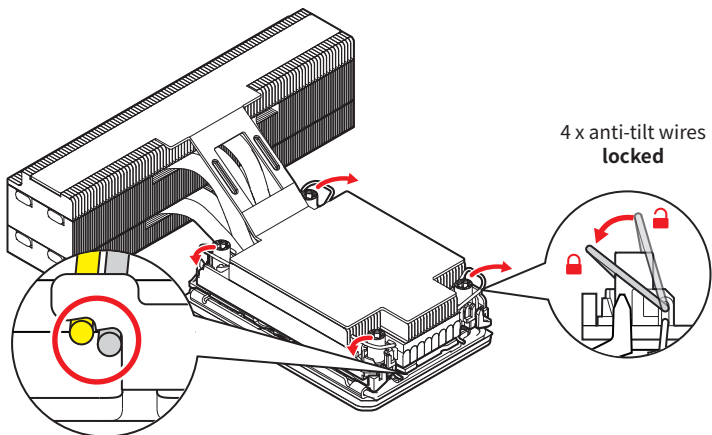
4. Check the heatsink for a diagonally cut corner or the #1 clip on the heatsink label if present. Align the **processor carrier's Pin 1 indicator** with the **heatsink's cut corner (#1 clip)**, then gently press the heatsink down to engage the carrier's latching mechanism to the heatsink at four corners.



5. Make sure the attached clips on the carrier grab onto the heatsink and firmly secure the carrier, CPU and heatsink as one **Processor Heatsink Module (PHM)**.
6. Remove the socket cover by squeezing the finger grips in, then flip **4 anti-tilt wires** on the heatsink to the **unlocked position (inward)** and place the PHM on top of the bolster plate with the Pin 1 indicators aligned. Hold the PHM horizontally, carefully lower down to engage PHM to bolster the plate's alignment pin.



7. Flip 4 anti-tilt wires to the **locked position (outward)** and make sure the wires are firmly secure.

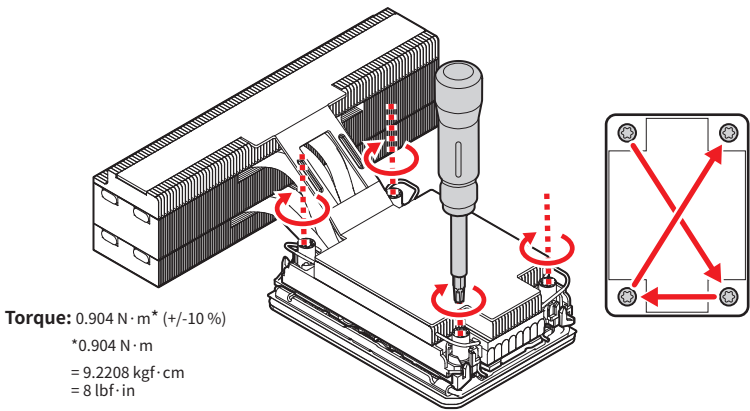


Important

Ensure the 4 anti-tilt wires rotate and lock into the **designated positions** on the stepped flanges, as specified in the table below for each CPU carrier.

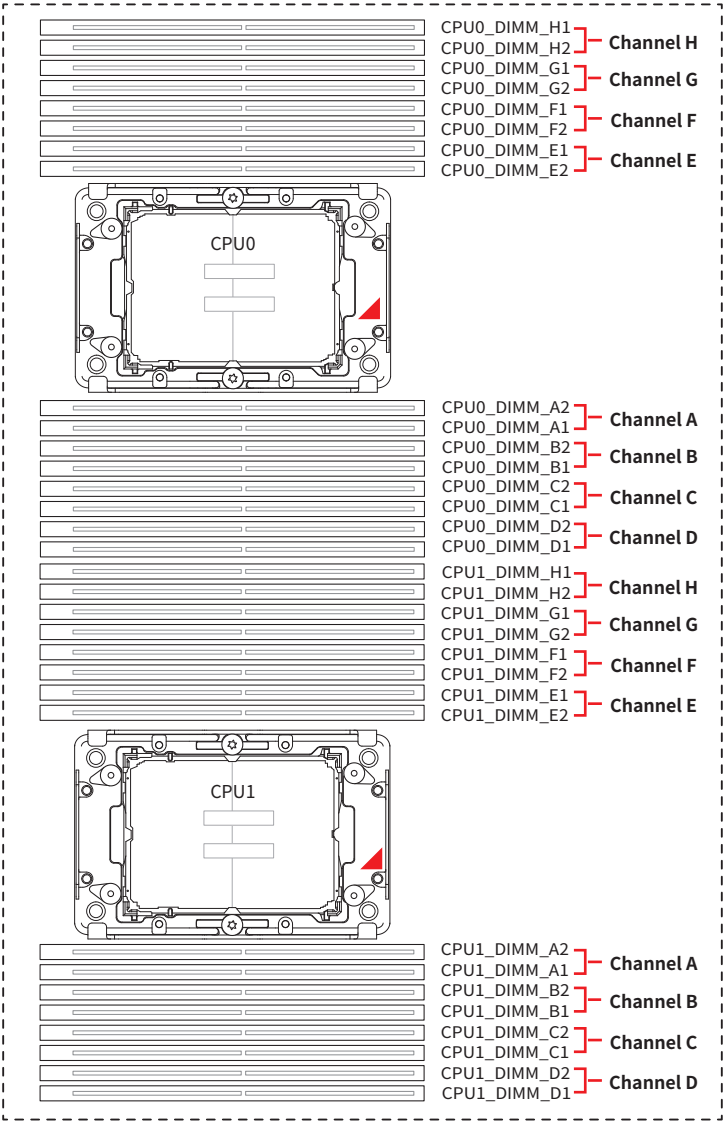
CPU Package Type	Thin Package	Thick Package
CPU Package Name	• Granite Rapids- SP XCC	• Granite Rapids- SP HCC/ LCC • Sierra Forest- SP
CPU Carrier Code	E2A	E2B
Anti-tilt Wire Position	 Lower step flange	 Upper step flange

8. Tighten all heatsink nuts using a **Torx T30 screwdriver** in a diagonal sequence to secure the PHM to the motherboard.
- To ensure even pressure on the CPU, first loosely fasten all four screws, then gradually tighten them.



Memory Slots

CPU0_DIMM_A1/A2~H1/H2,
CPU1_DIMM_A1/A2~H1/H2: DDR5 DIMM Slots



Recommended Memory Population



Please read the following Guidelines before populating memory.

General Memory Population Rules

- **Single DIMM Type Usage:** Only one type of DIMM is allowed across the system. Mixing different DIMM types is not permitted.
 - Example: All DDR5 RDIMMs or all MRDIMMs.
- **Consistent Rank Configuration:** All DIMMs within a channel must have the same number of ranks unless explicitly stated otherwise.
- **Uniform Speed:** All DDR5 DIMMs associated with a given processor (e.g., CPU0 or CPU1) must operate at the same speed.
- **Uniform Density:** All DDR5 DIMMs must have the same density.
- **Vendor Restrictions:** Unless explicitly stated otherwise, DIMMs from different vendors cannot be mixed for RDIMMs, 3DS RDIMMs, and MRDIMMs.

DIMM Mixing Restrictions

- Mixing of **non-3DS** and **3DS-RDIMMs** is not allowed in the same channel, across different channels, and across different processor sockets.
- **9x4 RDIMMs** cannot be mixed with other DIMM types.
- Mixing of DDR5 operating frequencies is not validated:
 - If DIMMs with varying maximum frequencies are mixed, the **BIOS determines and sets the DIMM speed** to the highest common frequency across all channels on the platform.
 - Example: If a 6000 MT/s DIMM is installed in one channel, and a 6400 MT/s DIMM in another, the BIOS sets the platform speed to 6000 MT/s.
- **x8 DIMMs and x4 DIMMs** cannot be mixed in the same channel or same processor socket. (Refer to the following "[DIMMs Population \(x4/x8\)](#)" section)

DIMMs Population (x4/x8)

Intel® Xeon® 6700E Series

DDR Type	DIMM population within IMC	
	Config Set A (x8)	Config Set B (x4)
	Slot 1, Slot 2	Slot 1, Slot 2
RDIMM	x8, None	x4, None x4, x4

Intel® Xeon® 6700P/ 6500P Series

DDR Type	DIMM population within IMC	
	Config Set A (x8)	Config Set B (x4)
	Slot 1, Slot 2	Slot 1, Slot 2
RDIMM	x8, None x8, x8	x4, None x4, x4
3DS-RDIMM		x4, None x4, x4
MRDIMM	x8, None	x4, None

Key Parameters for DIMM

Intel® Xeon® 6700E Series

DDR Type	Ranks Per DIMM & Data Width	DIMM Capacity (GB)						Speed (MT/s); Voltage (V); & DIMMs per Channel (DPC)	
		DRAM Density						1DPC	2DPC
		16 Gb		24 Gb		32 Gb		1.1 V	
		1DPC	2DPC	1DPC	2DPC	1DPC	2DPC		
RDIMM	1Rx4	32 GB						6400	5200
	2Rx8	32 GB							
	2Rx4	64 GB		96 GB		128 GB			

Intel® Xeon® 6700P/ 6500P Series

DDR Type	Ranks Per DIMM & Data Width	DIMM Capacity (GB)						Speed (MT/s); Voltage (V); & DIMMs per Channel (DPC)	
		DRAM Density						1DPC	2DPC
		16 Gb		24 Gb		32 Gb		1.1 V	
		1DPC	2DPC	1DPC	2DPC	1DPC	2DPC		
RDIMM	1Rx8	16 GB		24 GB				6400	6000
	1Rx4	32 GB		48 GB					
	2Rx8	32 GB		48 GB					
	2Rx4	64 GB		96 GB		128 GB			
3DS-RDIMM	8Rx4		256 GB					6400	6000
MRDIMM	2Rx8	32 GB						8000	
	2Rx4	64 GB							

DIMM Configuration

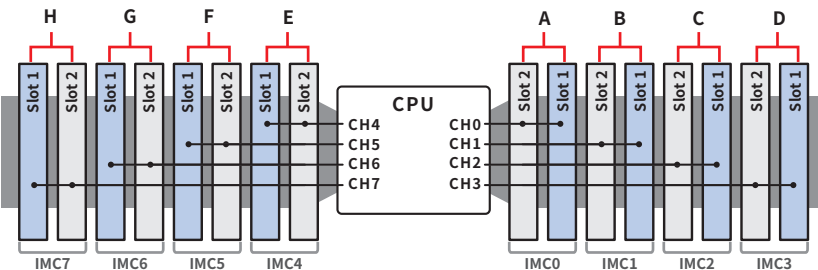
Intel® Xeon® 6700E Series

DDR Type	Memory Channels	Slots per Channel (SPC)	DIMMs per Channel (DPC)	Slot 1		Slot 2		DIMM Organization	DRAM Density (Gb)
				DIMM Ranks & Width	DIMM Capacity (GB)	DIMM Ranks & Width	DIMM Capacity (GB)		
RDIMM	8	1 or 2	1	2Rx8	32 GB			5x8	16 Gb
				1Rx4	32 GB			10x4	
				2Rx4	64 GB				
		2	2	2Rx4	64 GB	2Rx4	64 GB		
		1 or 2	1	2Rx4	96 GB			10x4	24 Gb
		2	2	2Rx4	96 GB	2Rx4	96 GB	10x4	24 Gb
		1 or 2	1	2Rx4	128 GB			10x4	32 Gb
		2	2	2Rx4	128 GB	2Rx4	128 GB	10x4	32 Gb

Intel® Xeon®6700P/ 6500P Series

DDR Type	Memory Channels	Slots per Channel (SPC)	DIMMs per Channel (DPC)	Slot 1		Slot 2		DIMM Organization	DRAM Density (Gb)		
				DIMM Ranks & Width	DIMM Capacity (GB)	DIMM Ranks & Width	DIMM Capacity (GB)				
RDIMM	4	1 or 2	1	2Rx8	32 GB			5x8	16 Gb		
					48 GB				24 Gb		
				2Rx4	64 GB			10x4	16 Gb		
	8	1 or 2	1	1Rx8	16 GB			5x8	16 Gb		
					24 GB				24 Gb		
				2Rx8	32 GB			5x8	16 Gb		
								10x4			
				1Rx4			10x4				
				2	2	2Rx8	32 GB	2Rx8	32 GB	5x8	16 Gb
				1 or 2	1.5	2Rx8	32 GB	2Rx8	32 GB	5x8	16 Gb
						2Rx8	48 GB			5x8	24 Gb
		1Rx4							10x4		
		2	2	2Rx8	48 GB	1Rx8	24 GB	5x8	24 Gb		
		1 or 2	1	2Rx4	64 GB			10x4	16 Gb		
					96 GB				24 Gb		
		2	2	2Rx4	64 GB	2Rx4	64 GB	10x4	16 Gb		
					96 GB		96 GB		24 Gb		
		1 or 2	1	2Rx4	128 GB			10x4	32 Gb		
		2	2		2Rx4	128 GB	2Rx4	128 GB	10x4	32 Gb	
					4H 3DS	256 GB	4H 3DS	256 GB		16 Gb	
MRDIMM	8	1 or 2	1	2Rx8	32 GB			5x8	16 Gb		
				2Rx4	64 GB			10x4			

DDR5 Only DIMM Configuration Diagram



IMC#	IMC7	IMC6	IMC5	IMC4	C P U	IMC0	IMC1	IMC2	IMC3
Channel	H	G	F	E		A	B	C	D
	Chan 7	Chan 6	Chan 5	Chan 4		Chan 0	Chan 1	Chan 2	Chan 3
	H1 H2	G1 G2	F1 F2	E1 E2		A2 A1	B2 B1	C2 C1	D2 D1
DDR5									
1						V			
4		V		V		V		V	
8	V	V	V	V		V	V	V	V
12	V	V	V	V		V	V	V	V
16	V	V	V	V		V	V	V	V

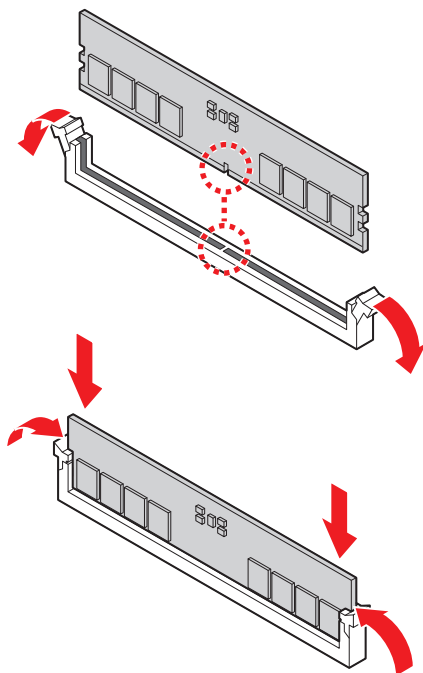
“V” indicates DIMMs are populated with DDR5.

 Important

- 1. Intel® Xeon® 6700E Series does not support 12 DIMMs configuration.
- 2. There should be at least one DDR5 DIMM per socket.
- 3. When only **one** DIMM is used in a channel, it must be populated in the **DIMM slot farthest away from the CPU (DIMM slot 1)** of a given channel.

Installing Memory Modules

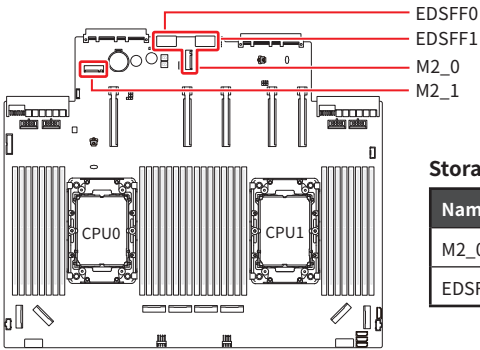
1. Open the side clips to unlock the DIMM slot.
2. Insert the DIMM vertically into the slot, ensuring that the off-center notch at the bottom aligns with the slot.
3. Push the DIMM firmly into the slot until it clicks and the side clips automatically close.
4. Verify that the side clips have securely locked the DIMM in place.



Important

You can barely see the golden finger if the memory module is properly inserted in the DIMM slot.

Storage Connectors



Storage Speed

Name	Description
M2_0~1	PCIe 5.0 x2, 32GT/s
EDSFF0~1 (E1.S)	PCIe 5.0 x4, 32GT/s

M2_0~1: M.2 Slots (M Key, 2280/ 22110)

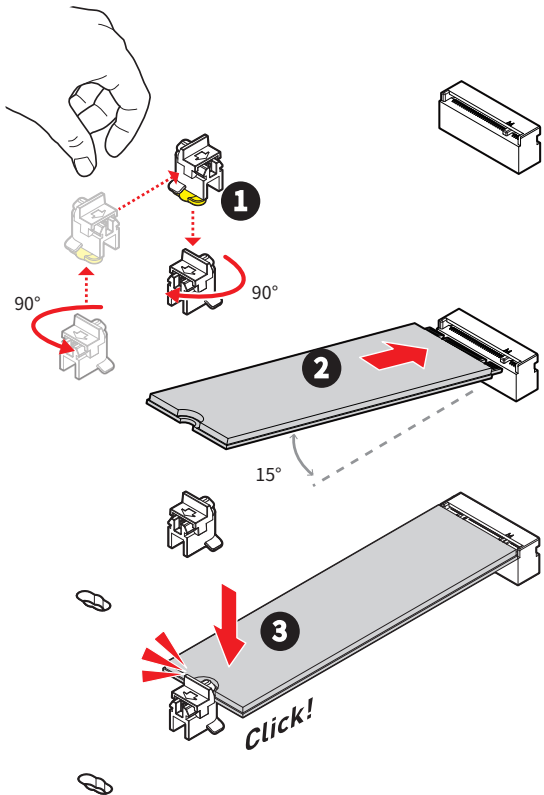
Please install the M.2 solid-state drive (SSD) into the M.2 slot as shown below.

1. Adjust the **M.2 board latch** to fit your M.2 SSD size.

- Turn the M.2 board latch **counterclockwise to release**, and **clockwise to lock**.

2. Insert your M.2 SSD into the M.2 slot at a 15-degree angle.

3. Push down the M.2 SSD till it clicks in place.

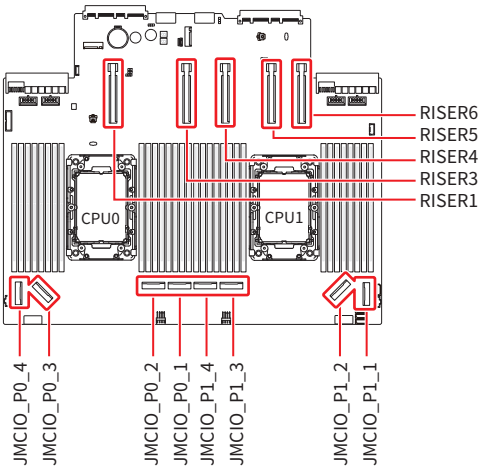


EDSFF0~1: E1.S 9.5mm Connectors

The connector supports EDSFF E1.S 9.5mm drives.

<div>EDSFF0~1</div> <div><div>B1B28</div><div><div>A1A28</div></div></div>	A1	GND	B1	P12V
	A2	GND	B2	P12V
	A3	GND	B3	P12V
	A4	GND	B4	P12V
	A5	GND	B5	P12V
	A6	GND	B6	P12V
	A7	EDSFF_PEHPCPU_SCL	B7	NC
	A8	EDSFF_PEHPCPU_SDA	B8	P3V3_AUX
	A9	RST_SMB_EDSFF	B9	EDSFF_DUALPORTEN#
	A10	FM_CPU0_EDSFF_LED_LVC3_BUFF	B10	RST_PCIE_PLRST_EDSFF-
	A11	RST_PLD_PERST_CLKREQN_OD	B11	P3V3_AUX
	A12	FM_CPU0_EDSFFX_PRSENT0_LVC3_N	B12	FM_CPU0_EDSFFX_PWRDIS_LVC3
	A13	GND	B13	GND
	A14	CLK_100M_EDSFF-	B14	CLK_100M_EDSFF-
	A15	CLK_100M_EDSFF+	B15	CLK_100M_EDSFF+
	A16	GND	B16	GND
	A17	P5E_CPU1_PE1_RX_D0-	B17	P5E_CPU1_PE1_TX_D0-
	A18	P5E_CPU1_PE1_RX_D0+	B18	P5E_CPU1_PE1_TX_D0+
	A19	GND	B19	GND
	A20	P5E_CPU1_PE1_RX_D1-	B20	P5E_CPU1_PE1_TX_D1-
	A21	P5E_CPU1_PE1_RX_D1+	B21	P5E_CPU1_PE1_TX_D1+
	A22	GND	B22	GND
	A23	P5E_CPU1_PE1_RX_D2-	B23	P5E_CPU1_PE1_TX_D2-
	A24	P5E_CPU1_PE1_RX_D2+	B24	P5E_CPU1_PE1_TX_D2+
	A25	GND	B25	GND
	A26	P5E_CPU1_PE1_RX_D3-	B26	P5E_CPU1_PE1_TX_D3-
	A27	P5E_CPU1_PE1_RX_D3+	B27	P5E_CPU1_PE1_TX_D3+
	A28	GND	B28	GND

Expansions



Expansions Speed

Name	Description
RISER1,3	PCIe 5.0 x16, 32 GT/s (from CPU0)
RISER4~6	PCIe 5.0 x16, 32 GT/s (from CPU1)
JMCIO_P0_1~4	PCIe 5.0 x8, 32 GT/s (from CPU0)
JMCIO_P1_1~4	PCIe 5.0 x8, 32 GT/s (from CPU1)

RISER1,3,4~6: SFF-TA-1033 M-XIO Slots

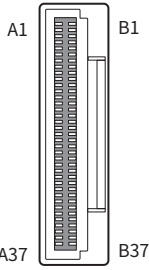
The SFF-TA-1033 M-XIO (Modular Hardware System Extensible I/O) slots support PCIe interfaces and are designed for flexible use with both cable and card-edge connections.

Important

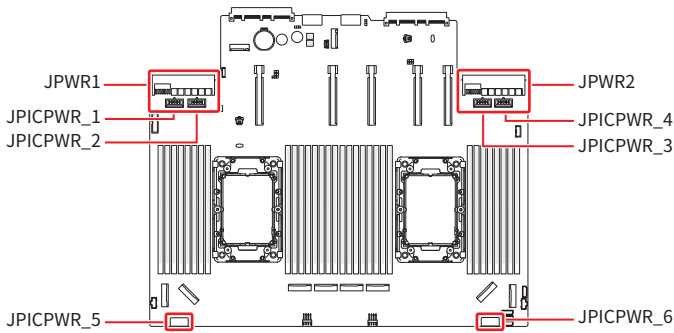
When adding or removing expansion cards, make sure that you unplug the power supply first. Meanwhile, read the documentation for the expansion card to configure any necessary hardware or software settings for the expansion card, such as jumpers, switches or BIOS configuration.

JMCIO_P0_1~4, JMCIO_P1_1~4: MCIO 8i Connectors

These are vertical 74-pin Mini Cool Edge IO (MCIO) connectors, which support PCIe 5.0 x8 32GT/s interface.

<div> JMCIO_P0_1~4 JMCIO_P1_1~4 </div> 	A1	GND	B1	GND
	A2	P5E_CPU_PE4_NVME_RX_D7+	B2	P5E_CPU_PE4_NVME_TX_D7+
	A3	P5E_CPU_PE4_NVME_RX_D7-	B3	P5E_CPU_PE4_NVME_TX_D7-
	A4	GND	B4	GND
	A5	P5E_CPU_PE4_NVME_RX_D6+	B5	P5E_CPU_PE4_NVME_TX_D6+
	A6	P5E_CPU_PE4_NVME_RX_D6-	B6	P5E_CPU_PE4_NVME_TX_D6-
	A7	GND	B7	GND
	A8	JMCIO_A8	B8	JMCIO_BMC_SCL
	A9	FM_SMB_PEHPCPU_MCIO_LVC3_ALERT_N	B9	JMCIO_BMC_SDA
	A10	GND	B10	GND
	A11	CLK_100M_CPU_MCIO_R_D+	B11	PCIe_RST1
	A12	CLK_100M_CPU_MCIO_R_D-	B12	FM_MCIO_CPU_PESTI_CBL_PRES_N
	A13	GND	B13	GND
	A14	P5E_CPU_PE4_NVME_RX_D5+	B14	P5E_CPU_PE4_NVME_TX_D5+
	A15	P5E_CPU_PE4_NVME_RX_D5-	B15	P5E_CPU_PE4_NVME_TX_D5-
	A16	GND	B16	GND
	A17	P5E_CPU_PE4_NVME_RX_D4+	B17	P5E_CPU_PE4_NVME_TX_D4+
	A18	P5E_CPU_PE4_NVME_RX_D4-	B18	P5E_CPU_PE4_NVME_TX_D4-
	A19	GND	B19	GND
	A20	P5E_CPU_PE4_NVME_RX_D3+	B20	P5E_CPU_PE4_NVME_TX_D3+
	A21	P5E_CPU_PE4_NVME_RX_D3-	B21	P5E_CPU_PE4_NVME_TX_D3-
	A22	GND	B22	GND
	A23	P5E_CPU_PE4_NVME_RX_D2+	B23	P5E_CPU_PE4_NVME_TX_D2+
	A24	P5E_CPU_PE4_NVME_RX_D2-	B24	P5E_CPU_PE4_NVME_TX_D2-
	A25	GND	B25	GND
	A26	SMB_MCIOP_CPU_SCL	B26	NC
	A27	SMB_MCIOP_CPU_SDA	B27	NC
	A28	GND	B28	GND
	A29	USB_HUB_MCIO_CPU_PE_D+	B29	FM_MCIO_CPU_FPGA_FLEXIO_1A
	A30	USB_HUB_MCIO_CPU_PE_D-	B30	FM_MCIO_CPU_FPGA_FLEXIO_2A
	A31	GND	B31	GND
	A32	P5E_CPU_PE4_NVME_RX_D1+	B32	P5E_CPU_PE4_NVME_TX_D1+
	A33	P5E_CPU_PE4_NVME_RX_D1-	B33	P5E_CPU_PE4_NVME_TX_D1-
	A34	GND	B34	GND
	A35	P5E_CPU_PE4_NVME_RX_D0+	B35	P5E_CPU_PE4_NVME_TX_D0+
	A36	P5E_CPU_PE4_NVME_RX_D0-	B36	P5E_CPU_PE4_NVME_TX_D0-
	A37	GND	B37	GND

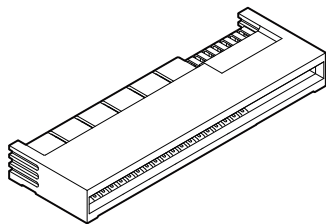
Power Connectors



JPWR1~2: CRPS/ M-CRPS 185x73.5mm Power Connectors

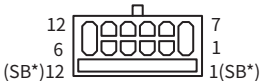
These connectors support both the **CRPS** (Common Redundant Power Supply) and **M-CRPS** (Modular Hardware System Common Redundant Power Supply) specifications, allowing for the connection of compatible power supplies.

To connect the power supply, ensure that the plug is correctly oriented and the pins are properly aligned with the connector. Once aligned, press the power supply firmly into place.



JPICPWR_1~6: 12-Pin PICPWR Power Connectors

The PICPWR (Platform Infrastructure Connectivity Power) connector enables the HPM (Host Processor Module) to supply power and manage sideband signals to peripherals, including **GPUs** (JPICPWR_1~4), the **storage backplane** (JPICPWR_5), and **fan board** (JPICPWR_6).

<div>JPICPWR_1~6</div> <div></div>	Power Signals			
	1	GND	7	+12V
	2	GND	8	+12V
	3	GND	9	+12V
	4	GND	10	+12V
	5	GND	11	+12V
	6	GND	12	+12V
	Sideband Management Signals			
	SB1	FM_HPM_PICPWR_B	SB7	FM_HPM_PICPWR_A
	SB2	FM_HPM_PICPWR_B	SB8	FM_HPM_PICPWR_A
	SB3**	SMB_PCIPWR_FANC_LVC3_SCL	SB9	NC
	SB4**	SMB_PCIPWR_FANC_LVC3_SDA	SB10	NC
	SB5	SMB_PICPWR_B_LVC3_SCL	SB11	SMB_PICPWR_A_LVC3_SCL
	SB6	SMB_PICPWR_B_LVC3_SDA	SB12	SMB_PICPWR_A_LVC3_SDA

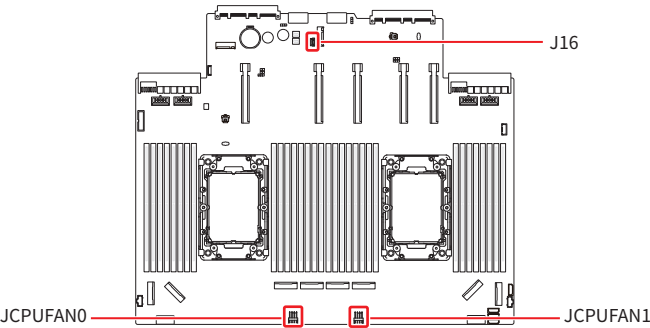
***SB:** The term “SB” stands for sideband.

****SB3 & SB4:** The sideband signals SB3 and SB4 are functional only for the **JPICPWR_5** connector. For JPICPWR_1, JPICPWR_2, JPICPWR_3, JPICPWR_4, and JPICPWR_6, these signals have **no connection (NC)**.



Make sure that all power connectors are securely connected to the power supply to ensure stable operation of the motherboard.

Cooling Connectors



JCPUFAN0~1: 4-Pin Fan Connectors (debug only)

The fan connector supports cooling fans with +12V. When connecting the wire to the connectors, always note that the red wire is the positive and should be connected to the +12V; the black wire is Ground and should be connected to GND.

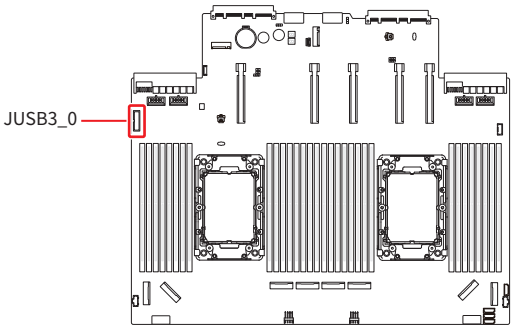
<div>JCPUFAN0~1</div> 	1	GND
	2	+12V
	3	NC
	4	NC

J16: Liquid Leak Detection Connector

This connector is for detecting water leaks in the CPU liquid cooling pump. If a leak is detected, the system will automatically shut down for protection.

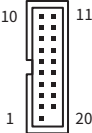
<div>J16</div> 	1	GND
	2	P12V_AUX
	3	FM_LIQUID_INT_N
	4	FM_DTECTOR_PRESENT_N

USB Connectors



JUSB3_0: USB 3.2 Gen 1 Connector

The USB (Universal Serial Bus) port is for attaching USB devices such as keyboard, mouse, or other USB-compatible devices. It supports up to **5Gbps** and backward compatibility with USB 2.0 devices (**480 Mbps**).

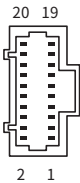
<div>JUSB3_0</div> 	1	P5V_USB_1	11	USB2_P3_ESD_D+
	2	USB3_P2_ESD_RX-	12	USB2_P3_ESD_D-
	3	USB3_P2_ESD_RX+	13	GND
	4	GND	14	USB3_P3_ESD_TX+
	5	USB3_P2_ESD_TX-	15	USB3_P3_ESD_TX-
	6	USB3_P2_ESD_TX+	16	GND
	7	GND	17	USB3_P3_ESD_RX+
	8	USB2_P2_ESD_D-	18	USB3_P3_ESD_RX-
	9	USB2_P2_ESD_D+	19	P5V_USB_2
	10	NC	20	No Pin

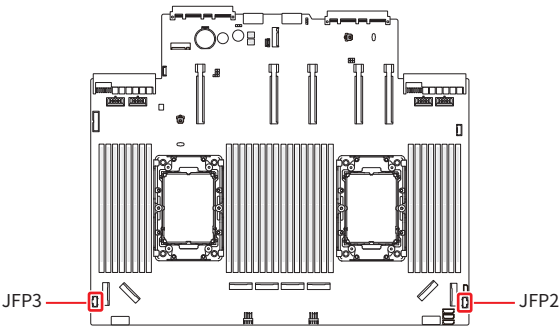
Other Connectors and Components

JFP2~3: DC-MHS Control Panel Header

The **DC-MHS** control panel header for **M-PESTI** connects the **HPM** to the server's front panel, enabling essential controls such as power, LED indicators, buttons, and sideband signals for management and monitoring.

- **DC-MHS (Data Center Modular Hardware System)** is a modular framework for data center hardware, promoting interoperability across components.
- **M-PESTI (Modular Hardware System Peripheral Sideband Tunneling Interface)** standardizes communication for peripheral components, allowing automatic discovery and configuration.
- **HPM (Host Processor Module)** is the main processing module in a server, responsible for managing power, control signals, and peripheral interfaces.

<div>JFP2~3</div> <div></div>	1	P12V_AUX	2	GND
	3	P12V_AUX	4	BMC_SMB_LVC3_PESTI1_SDA
	5	NC	6	BMC_SMB_LVC3_PESTI1_SCL
	7	GND	8	GND
	9	USB2_BMC_PCP_ESD_D+	10	FM_FP_HPM_PCP_SB4
	11	USB2_BMC_PCP_ESD_D-	12	FM_FP_HPM_PCP_SB3
	13	GND	14	FM_FP_HPM_PCP_SB2
	15	SPI_BMC_FP_MISO_R	16	FM_FP_HPM_PCP_SB1
	17	SPI_BMC_FP_CS0_R	18	GND
	19	SPI_BMC_FP_MOSI_R	20	SPI_BMC_FP_CK_R



JRST_P1: Reset Button Header

This header is provided to connect the system reset button.

JRST_P1		1	1	FM_RST_BTN_CPU1_LVC18_N
			2	GND

JPWR_P1: Power Button Header

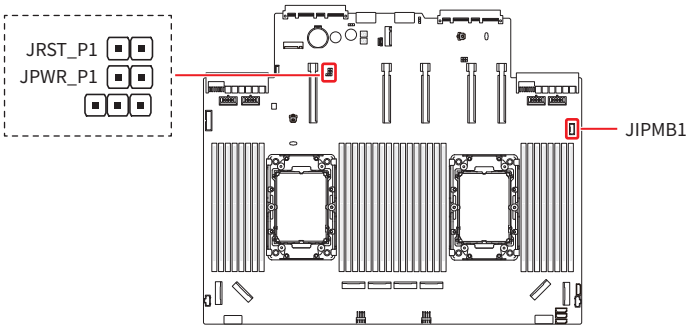
This header is provided to connect the system power button.

JPWR_P1		1	1	FM_PWR_BTN_CPU1_LVC18_N
			2	GND

J_IPMB1: IPMB Header

This header is used to connect the Intelligent Platform Management Bus.

J_IPMB1		1	1	SMB_IPMB_STBY_CMOS_ISO_SDA
			2	GND
			3	SMB_IPMB_STBY_CMOS_ISO_SCL
			4	P5V_AUX



JVROC1: VROC Connector

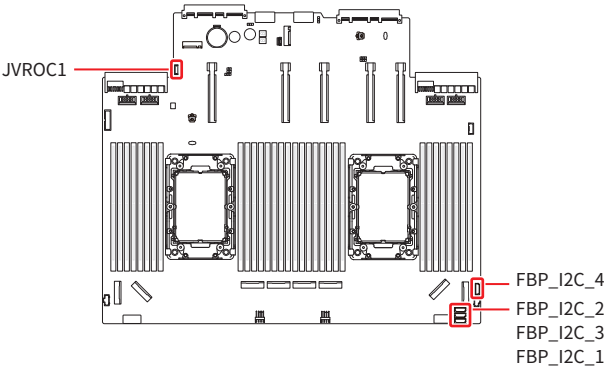
Intel® Virtual RAID on CPU (Intel® VROC) is a hybrid RAID solution specifically designed for NVMe SSDs connected directly to the CPU.

<div>JVROC1</div> <div><div>1</div><div>4</div></div>	1	GND
	2	PU_KEY_CONN_PIN2_R
	3	GND
	4	FM_PCH_SATA_RAID_KEY_R

FBP_I2C_1~4: I2C Headers

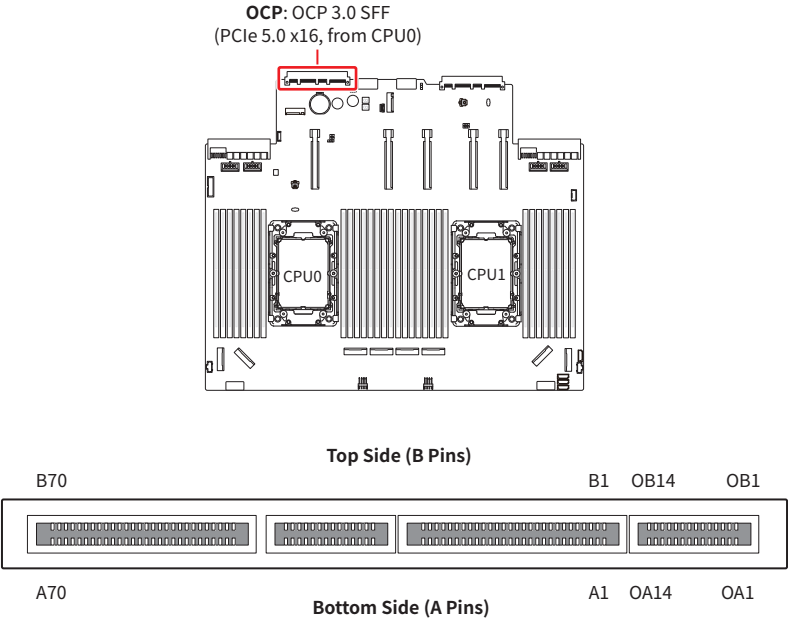
I²C (Inter-Integrated Circuit) headers connect to the System Management Bus (SMBus), **FBP_I2C_1~3** are for the hot-swap backplane; **FBP_I2C_4** is for thermal functions.

<div>FBP_I2C_1~4</div> <div><div>4</div><div>1</div></div>	1	P3V3
	2	SMB_HSBP_LVC3_R_SCL
	3	SMB_HSBP_LVC3_R_SDA
	4	GND



OCP: OCP 3.0 Mezzanine Slot

This slot enables the deployment of a wide variety of additional options through OCP (Open Compute Project) network interface cards (NICs) or other expansion cards.



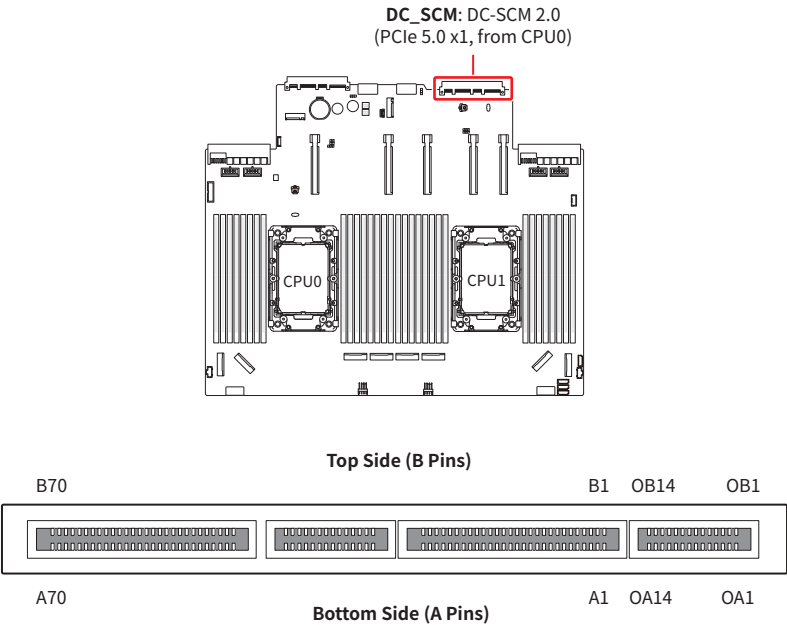
Top Side (B Pins)		Bottom Side (A Pins)	
OB1	PWRGD_OCP1_NIC1_PWRGD_R	OA1	RST_CPU0_PE3_OCP1_PERST2_N
OB2	FM_OCP_NIC_MAIN_PWR_EN	OA2	RST_CPU0_PE3_OCP1_PERST3_N
OB3	OCP1_NIC_LD_N	OA3	IRQ_WAKE_CPU0_PE3_OCP1_LVC3_N
OB4	OCP1_DATA_IN	OA4	OCP1_RBT_ARB_IN
OB5	OCP1_NIC_DATA_OUT	OA5	OCP1_RBT_ARB_OUT
OB6	OCP1_NIC_CLK	OA6	PUD_OCP1_SLOT_ID1_N
OB7	PUD_OCP1_SLOT_ID0_N	OA7	RMII3_SCM_TX_EN_R
OB8	RMII3_SCM_RXD1	OA8	RMII3_SCM_TXD1
OB9	RMII3_SCM_RXD0	OA9	RMII3_SCM_TXD0
OB10	GND-1	OA10	GND-50
OB11	NC	OA11	NC
OB12	NC	OA12	NC
OB13	GND-2	OA13	GND-49
OB14	RMII3_SCM_CRD_DV_R	OA14	CLK_50M_OCP1

Top Side (B Pins)		Bottom Side (A Pins)	
Mechanical Key			
B1	+12V_EDGE-1	A1	GND-48
B2	+12V_EDGE-2	A2	GND-47
B3	+12V_EDGE-3	A3	GND-46
B4	+12V_EDGE-4	A4	GND-45
B5	+12V_EDGE-5	A5	GND-44
B6	+12V_EDGE-6	A6	GND-43
B7	PD_OCP1_NIC_BIF0_N	A7	SMB_CPU0_PE3_OCP1_LVC3_SCL
B8	PD_OCP1_NIC_BIF1_N	A8	SMB_CPU0_PE3_OCP1_LVC3_SDA
B9	PD_OCP1_NIC_BIF2_N	A9	RST_BMC_PCIE_MUX_R_LVC3_N
B10	PERST0#	A10	PD_CPU0_OCP1_NIC_PRSNTA_N
B11	P3V3_AUX	A11	RST_CPU0_PE3_OCP1_PERST1_N
B12	FM_OCP_NIC_AUX_PWR_LVC3_R_EN	A12	FM_CPU0_OCP1_NIC_PRSNTB2_N
B13	GND-3	A13	GND-42
B14	CLK_100M_CPU0_OCP1_0_DN	A14	CLK_100M_CPU0_OCP1_1_DN
B15	CLK_100M_CPU0_OCP1_0_DP	A15	CLK_100M_CPU0_OCP1_1_DP
B16	GND-4	A16	GND-41
B17	P5E_CPU0_PE3_OCP_TX_DN15	A17	P5E_CPU0_PE3_OCP_RX_DN15
B18	P5E_CPU0_PE3_OCP_TX_DP15	A18	P5E_CPU0_PE3_OCP_RX_DP15
B19	GND-5	A19	GND-40
B20	P5E_CPU0_PE3_OCP_TX_DN14	A20	P5E_CPU0_PE3_OCP_RX_DN14
B21	P5E_CPU0_PE3_OCP_TX_DP14	A21	P5E_CPU0_PE3_OCP_RX_DP14
B22	GND-6	A22	GND-39
B23	P5E_CPU0_PE3_OCP_TX_DN13	A23	P5E_CPU0_PE3_OCP_RX_DN13
B24	P5E_CPU0_PE3_OCP_TX_DP13	A24	P5E_CPU0_PE3_OCP_RX_DP13
B25	GND-7	A25	GND-38
B26	P5E_CPU0_PE3_OCP_TX_DN12	A26	P5E_CPU0_PE3_OCP_RX_DN12
B27	P5E_CPU0_PE3_OCP_TX_DP12	A27	P5E_CPU0_PE3_OCP_RX_DP12
B28	GND-8	A28	GND-37
Mechanical Key			
B29	GND-9	A29	GND-36
B30	P5E_CPU0_PE3_OCP_TX_DN11	A30	P5E_CPU0_PE3_OCP_RX_DN11
B31	P5E_CPU0_PE3_OCP_TX_DP11	A31	P5E_CPU0_PE3_OCP_RX_DP11
B32	GND-10	A32	GND-35
B33	P5E_CPU0_PE3_OCP_TX_DN10	A33	P5E_CPU0_PE3_OCP_RX_DN10
B34	P5E_CPU0_PE3_OCP_TX_DP10	A34	P5E_CPU0_PE3_OCP_RX_DP10
B35	GND-11	A35	GND-34
B36	P5E_CPU0_PE3_OCP_TX_DN9	A36	P5E_CPU0_PE3_OCP_RX_DN9
B37	P5E_CPU0_PE3_OCP_TX_DP9	A37	P5E_CPU0_PE3_OCP_RX_DP9
B38	GND-12	A38	GND-33
B39	P5E_CPU0_PE3_OCP_TX_DN8	A39	P5E_CPU0_PE3_OCP_RX_DN8

Top Side (B Pins)		Bottom Side (A Pins)	
B40	P5E_CPU0_PE3_OCP_TX_DP8	A40	P5E_CPU0_PE3_OCP_RX_DP8
B41	GND-13	A41	GND-32
B42	FM_CPU0_OCP1_NIC_PRSNTB0_N	A42	FM_CPU0_OCP1_NIC_PRSNTB1_N
Mechanical Key			
B43	GND-14	A43	GND-31
B44	P5E_CPU0_PE3_OCP_TX_DN7	A44	P5E_CPU0_PE3_OCP_RX_DN7
B45	P5E_CPU0_PE3_OCP_TX_DP7	A45	P5E_CPU0_PE3_OCP_RX_DP7
B46	GND-15	A46	GND-30
B47	P5E_CPU0_PE3_OCP_TX_DN6	A47	P5E_CPU0_PE3_OCP_RX_DN6
B48	P5E_CPU0_PE3_OCP_TX_DP6	A48	P5E_CPU0_PE3_OCP_RX_DP6
B49	GND-16	A49	GND-29
B50	P5E_CPU0_PE3_OCP_TX_DN5	A50	P5E_CPU0_PE3_OCP_RX_DN5
B51	P5E_CPU0_PE3_OCP_TX_DP5	A51	P5E_CPU0_PE3_OCP_RX_DP5
B52	GND-17	A52	GND-28
B53	P5E_CPU0_PE3_OCP_TX_DN4	A53	P5E_CPU0_PE3_OCP_RX_DN4
B54	P5E_CPU0_PE3_OCP_TX_DP4	A54	P5E_CPU0_PE3_OCP_RX_DP4
B55	GND-18	A55	GND-27
B56	P5E_CPU0_PE3_OCP_TX_DN3	A56	P5E_CPU0_PE3_OCP_RX_DN3
B57	P5E_CPU0_PE3_OCP_TX_DP3	A57	P5E_CPU0_PE3_OCP_RX_DP3
B58	GND-19	A58	GND-26
B59	P5E_CPU0_PE3_OCP_TX_DN2	A59	P5E_CPU0_PE3_OCP_RX_DN2
B60	P5E_CPU0_PE3_OCP_TX_DP2	A60	P5E_CPU0_PE3_OCP_RX_DP2
B61	GND-20	A61	GND-25
B62	P5E_CPU0_PE3_OCP_TX_DN0	A62	P5E_CPU0_PE3_OCP_RX_DN1
B63	P5E_CPU0_PE3_OCP_TX_DP0	A63	P5E_CPU0_PE3_OCP_RX_DP1
B64	GND-21	A64	GND-24
B65	P5E_CPU0_PE3_OCP_TX_DN0	A65	P5E_CPU0_PE3_OCP_RX_DN0
B66	P5E_CPU0_PE3_OCP_TX_DP0	A66	P5E_CPU0_PE3_OCP_RX_DP0
B67	GND-22	A67	GND-23
B68	P3V3_AUX	A68	USB2_OCP_NIC_DN
B69	NC	A69	USB2_OCP_NIC_DP
B70	FM_CPU0_OCP1_NIC_PRSNTB3_N	A70	FM_PWRBRK_CPU0_PE3_OCP1_LVC3_N

DC-SCM: DC-SCM 2.0 Edge Slot

The slot links the **Datacenter Secure Control Module (DC-SCM)** to the motherboard, enabling centralized power, management, and security control across server hardware. This standardized interface allows easy upgrades and compatibility across various platforms.



Top Side (B Pins)		Bottom Side (A Pins)	
OB1	GND-1	OA1	GND-17
OB2	NC	OA2	NC
OB3	NC	OA3	NC
OB4	GND-2	OA4	GND-18
OB5	NC	OA5	NC
OB6	NC	OA6	NC
OB7	GND-3	OA7	GND-19
OB8	NC	OA8	NC
OB9	NC	OA9	NC
OB10	GND-4	OA10	GND-20
OB11	USB2_BMC_HUB_DN	OA11	NC
OB12	USB2_BMC_HUB_DP	OA12	NC
OB13	GND-5	OA13	GND-21
OB14	P1V0_AUX	OA14	PECI_SCM_R

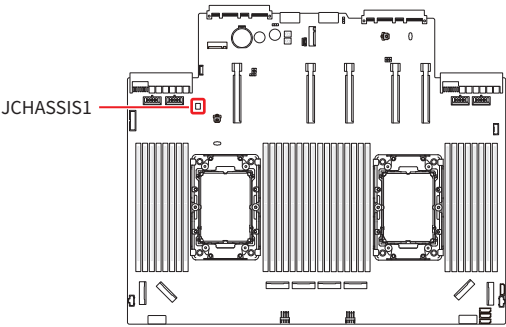
Top Side (B Pins)		Bottom Side (A Pins)	
Mechanical Key			
B1	CLK_66M_ESPI_CPU0_LVC18	A1	P12V_AUX
B2	ESPI_CPU0_CS0_SCM_N	A2	P12V_AUX_1
B3	RST_ESPI_CPU0_LVC18_N	A3	P12V_AUX_2
B4	ESPI_CPU0_IO0_LVC18	A4	P12V_AUX_3
B5	ESPI_CPU0_IO1_LVC18	A5	P12V_AUX_4
B6	ESPI_CPU0_IO2_LVC18	A6	GND-22
B7	ESPI_CPU0_IO3_LVC18	A7	GND-23
B8	IRQ_ESPI_CPU0_ALERT0_FPGA_LVC18_N	A8	BMC_JTAG_LVC3_TCK
B9	NC	A9	BMC_JTAG_LVC3_TDI
B10	NC	A10	BMC_JTAG_LVC3_TDO
B11	GND-6	A11	BMC_JTAG_LVC3_TMS
B12	SPI_CPU0_CLK_DCSCM_LVC18_R1	A12	NC
B13	SPI_CPU0_CS0_DCSCM_LVC18_R1_N	A13	FM_HPM_STBY_RST_N
B14	SPI_CPU0_IO0_DCSCM_LVC18_R1	A14	FM_HPM_STBY_EN
B15	SPI_CPU0_IO1_DCSCM_LVC18_R1	A15	SMB_CHASSIS_SENSOR_STBY_LVC3_SCL
B16	SPI_CPU0_IO2_DCSCM_LVC18_R1	A16	SMB_CHASSIS_SENSOR_STBY_LVC3_SDA
B17	SPI_CPU0_IO3_DCSCM_LVC18_R1	A17	SMB_HSBP_SCM_LVC3_R_SCL
B18	SPI_CPU0_CS1_DCSCM_LVC18_R1_N	A18	SMB_HSBP_SCM_LVC3_R_SDA
B19	GND-7	A19	GND-24
B20	LVDS_LVC18_TX_DN	A20	LVDS_LVC18_RX_DN
B21	LVDS_LVC18_TX_DP	A21	LVDS_LVC18_RX_DP
B22	GND-6	A22	GND-25
B23	LVDS_LVC18_CLK_TX_DN	A23	LVDS_LVC18_CLK_RX_DN
B24	LVDS_LVC18_CLK_TX_DP	A24	LVDS_LVC18_CLK_RX_DP
B25	GND-7	A25	GND-26
B26	FM_HPM_STBY_RDY	A26	SMB_PMBUS2_LVC3_SCL
B27	FM_INTRUDER_HDR_BMC_N	A27	SMB_PMBUS2_LVC3_SDA
B28	P3V_BAT_CPU0	A28	RST_PLD_PCIE_CPU0_DEV_PERST_N
Mechanical Key			
B29	GND-10	A29	GND-27
B30	P5E_CPU0_PE1_TX_DN2	A30	P5E_CPU0_PE1_RX_DN2
B31	P5E_CPU0_PE1_TX_DP2	A31	P5E_CPU0_PE1_RX_DP2
B32	GND-11	A32	GND-28
B33	HUB_SSTX1N	A33	HUB_SSRX1N
B34	HUB_SSTX1P	A34	HUB_SSRX1P
B35	GND-12	A35	GND-29
B36	USB2_P1_DN	A36	CLK_100M_SCM_DN
B37	USB2_P1_DP	A37	CLK_100M_SCM_DP
B38	GND-13	A38	GND-30
B39	I3C_DBG_SCM_LVC18_R_SCL	A39	I3C_SPD_SCM_R_LVC1_SCL
B40	I3C_DBG_SCM_LVC18_R_SDA	A40	I3C_SPD_SCM_R_LVC1_SDA

Top Side (B Pins)		Bottom Side (A Pins)	
B41	NC	A41	I3C_MNG_SCM_LVC1_R_SCL
B42	NC	A42	I3C_MNG_SCM_LVC1_R_SDA
Mechanical Key			
B43	CLK3_50M_SCM_RMII_CLK	A43	SMB_PCIE_SCM_LVC3_R_SCL
B44	RMII3_SCM_CRD_V_R_DC	A44	SMB_PCIE_SCM_LVC3_R_SDA
B45	RMII3_SCM_TX_EN_R_DC	A45	SMB_IPMB_LVC3_CLK
B46	RMII3_SCM_TXD0_DC	A46	SMB_IPMB_LVC3_DAT
B47	RMII3_SCM_TXD1_DC	A47	SMB_CPLD_UPDATE_SCM_LVC3_R_SCL
B48	RMII3_SCM_RXD0_DC	A48	SMB_CPLD_UPDATE_SCM_LVC3_R_SDA
B49	RMII3_SCM_RXD1_DC	A49	SMB_PMBUS1_LVC3_SCL
B50	NC	A50	SMB_PMBUS1_LVC3_SDA
B51	UART0_TX_SCM_HPM_DATA	A51	BMC_SMB_LVC18_CLK1
B52	SMB_HOST_STBY_LVC3_SCL	A52	BMC_SMB_LVC18_DAT1
B53	SMB_HOST_STBY_LVC3_SDA	A53	GND-31
B54	DBP_ASD_SCM_PREQ_LVC3_R_N	A54	SPI_CPU0_TPM_CLK_LVC18_MUX_R1
B55	DBP_ASD_SCM_PRDY_LVC3_R_N	A55	SPI_CPU0_TPM_CS_LVC18_MUX_R1_N
B56	SMB16_IPMB_LVC3_SCL	A56	SPI_CPU0_TPM_MOSI_LVC18_MUX_R1
B57	SMB16_IPMB_LVC3_SDA	A57	SPI_CPU0_TPM_MISO_LVC18_MUX_R1
B58	FM_SCM_PRSTNT0_LVC3_N	A58	NC
B59	NC	A59	NC
B60	SPI_BMC_FP_CHK_R	A60	IRQ_CPU0_TPM_N
B61	SPI_BMC_FP_MISO_R	A61	SMB_HOST_P1_STBY_LVC18_SCL
B62	SPI_BMC_FP_MOSI_R	A62	SMB_HOST_P1_STBY_LVC18_SDA [
B63	SPI_BMC_FP_CS0_R	A63	UART0_RX_HPM_SCM_DATA
B64	GND-14	A64	GND-32
B65	NC	A65	NC
B66	NC	A66	NC
B67	GND-15	A67	GND-33
B68	USB2_P4_DN	A68	NC
B69	USB2_P4_DP	A69	NC
B70	GND-16	A70	GND-34

JCHASSIS1: Chassis Intrusion Header

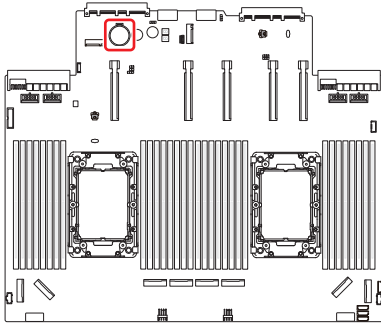
This header connects to the **chassis intrusion switch cable**, which monitors and detects any unauthorized opening in the server's chassis. When the chassis is opened, this header sends a signal to notify the **Baseboard Management Controller (BMC)** to record the intrusion event or trigger an alert for administrators.

JCHASSIS1		1	P3V3_AUX
		2	GND
		3	FM_INTRUDER_HDR_BMC_N



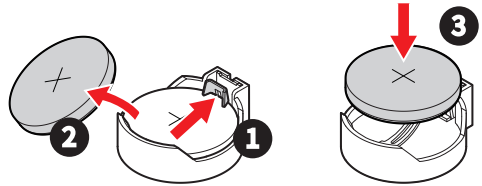
BAT1: CMOS Battery

If the CMOS battery is out of charge, the time in the BIOS will be reset and the data of system configuration will be lost. In this case, you need to replace the CMOS battery.



Replacing CMOS battery

1. Push the retainer clip to free the battery.
2. Remove the battery from the socket.
3. Install the new CR2032 coin-cell battery with the + sign facing up. Ensure that the retainer holds the battery securely.



WARNING

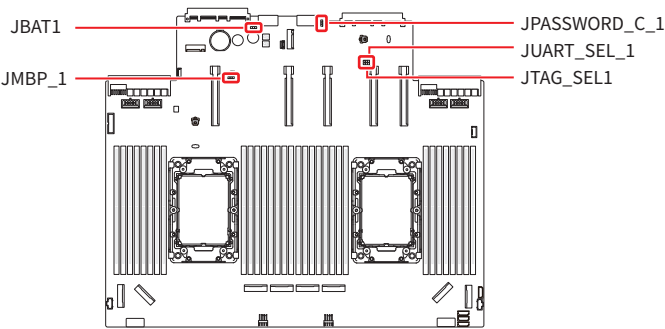
KEEP OUT OF REACH OF CHILDREN

- Swallowing can cause chemical burns, perforation of soft tissue, and even death.
- Severe burns can occur within 2 hours of ingestion.
- If you think batteries might have been swallowed or placed inside any part of the body, seek immediate medical attention.

Jumpers



Avoid adjusting jumpers when the system is on; it will damage the motherboard.

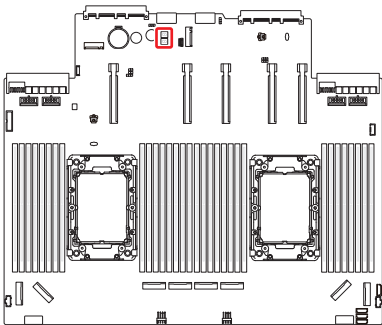


Jumper Name	Default Setting	Description
JMBP_1	 1	MBP/ I3C MIPI Mode Select Jumper
		1-2: MBP Mode (default)
		2-3: I3C MIPI Mode
JBAT1	 1	CMOS Clear Jumper
		1-2: Normal (default)
		2-3: Clear CPU0 CMOS
JPASSWORD_C_1	 1	Password Clear Jumper
		1-2: Normal (default)
		2-3: Clear password
JUART_SEL1	 1	UART BMC/ CPLD Select Jumper
		1-2: UART BMC to CPU (default)
		2-3: UART CPLD to CPU
JTAG_SEL1	 1	JTAG Select Jumper
		1-2: BMC to CPLD (default)
		2-3: BMC to CPU

Onboard LEDs

LED_H1, LED_L1: Port 80 Debug LEDs

The Port 80 Debug LEDs display progress and error codes during and after POST (Power-On Self Test).



Hexadecimal Character Table

Hexadecimal	0	1	2	3	4	5	6	7
LED display	0	1	2	3	4	5	6	7
Hexadecimal	8	9	A	B	C	D	E	F
LED display	8	9	A	b	C	d	E	F

Regulatory Notices

CE Conformity

This product has been tested and found to comply with the harmonized standards for Information Technology Equipment published under Directives of Official Journal of the European Union.



FCC-A Radio Frequency Interference Statement

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.



Notice 1

The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Notice 2

Shielded interface cables and AC power cord, if any, must be used in order to comply with the emission limits.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference, and
- This device must accept any interference received, including interference that may cause undesired operation.

Battery Information

Please take special precautions if this product comes with a battery.

- Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer.
- Avoid disposal of a battery into fire or a hot oven, or mechanically crushing or cutting of a battery, which can result in an explosion.
- Avoid leaving a battery in an extremely high temperature or extremely low air pressure environment that can result in an explosion or the leakage of flammable liquid or gas.
- Do not ingest battery. If the coin/button cell battery is swallowed, it can cause severe internal burns and can lead to death. Keep new and used batteries away from children.

European Union:



Batteries, battery packs, and accumulators should not be disposed of as unsorted household waste. Please use the public collection system to return, recycle, or treat them in compliance with the local regulations.

BSMI:



廢電池請回收

For better environmental protection, waste batteries should be collected separately for recycling or special disposal.

California, USA:



The button cell battery may contain perchlorate material and requires special handling when recycled or disposed of in California. For further information please visit:

<http://www.dtsc.ca.gov/hazardouswaste/perchlorate/>

RoHS Statement

日本JIS C 0950材質宣言

日本工業規格JIS C 0950により、2006年7月1日以降に販売される特定分野の電気および電子機器について、製造者による含有物質の表示が義務付けられます。

<https://csr.msi.com/tw/Japan-JIS-C-0950-Material-Declarations>

India RoHS

This product complies with the “India E-waste (Management and Handling) Rule 2016” and prohibits use of lead, mercury, hexavalent chromium, polybrominated biphenyls or polybrominated diphenyl ethers in concentrations exceeding 0.1 weight % and 0.01 weight % for cadmium, except for the exemptions set in Schedule 2 of the Rule.

Türkiye EEE yönetmeliği

Türkiye Cumhuriyeti: EEE Yönetmeliğine Uygundur

Україна обмеження на наявність небезпечних речовин

Обладнання відповідає вимогам Технічного регламенту щодо обмеження використання деяких небезпечних речовин в електричному та електронному обладнанні, затвердженого постановою Кабінету Міністрів України від 10 березня 2017 р. № 139

Việt Nam RoHS

Kể từ ngày 01/12/2012, tất cả các sản phẩm do công ty MSI sản xuất tuân thủ Thông tư số 30/2011/TT-BCT quy định tạm thời về giới hạn hàm lượng cho phép của một số hóa chất độc hại có trong các sản phẩm điện, điện tử”

Bangladesh RoHS Statement

This product shipping to Bangladesh comply with RoHS requirements as prescribed in the Hazardous Waste (E-waste) Management Rules, 2021 by Government of Bangladesh.

For more information, please refer:

<https://csr.msi.com/global/bangladesh-rohs-statement>

Bangladesh E-waste Management Reminder

Please manage, dismantle, dispose of, or recycle e-waste properly as per the Environmental Protection Rules, 1997 to avoid the harm that may be caused to the environment and ecosystem, public interest and public health.

Material Declaration under India’ s Plastic Waste Management Rules:

INDOMSI COMPUTERS PRIVATE LIMITED

Regn. No.: IM-06-000-06-AAHCI0478A-25

Thickness ≥ 50 microns

限用物質含有情況標示聲明書

單元	限用物質及其化學符號					
	鉛 (Pb)	汞 (Hg)	鎘 (Cd)	六價鉻 (Cr ⁶⁺)	多溴聯苯 (PBB)	多溴二苯醚 (PBDE)
電路板	—	○	○	○	○	○
電子元件	—	○	○	○	○	○
金屬機構件	—	○	○	○	○	○
塑膠機構件	○	○	○	○	○	○
配件(例:電源線等)	—	○	○	○	○	○
備考1. “超出0.1 wt %”及“超出0.01 wt %”係指限用物質之百分比含量超出百分比含量基準值。						
備考2. “○”係指該項限用物質之百分比含量未超出百分比含量基準值。						
備考3. “—”係指該項限用物質為排除項目。						

产品中有害物质的名称及含有信息表

部件名称	有害物质									
	Pb	Hg	Cd	Cr(VI)	PBBs	PBDEs	DBP	DIBP	BBP	DEHP
电路板组件*	×	○	○	○	○	○	○	○	○	○
处理器和散热器	×	○	○	○	○	○	○	○	○	○
内存条/硬盘	×	○	○	○	○	○	○	○	○	○
电缆/连接器	×	○	○	○	○	○	○	○	○	○
金属机构件	×	○	○	○	○	○	○	○	○	○
注1：○：表示该有害物质在该部件所有均质材料中的含量均不超出电器电子产品有害物质限制使用国家标准要求。										
×：表示该有害物质至少在该部件的某一均质材料中的含量超出电器电子产品有害物质限制使用国家标准要求。										
注2：以上未列出的部件，表明其有害物质含量均不超出电器电子产品有害物质限制使用国家标准要求。										
注3：上述表格标注“×”之部件，皆符合达标管理目录限用物质应用例外清单之限值要求。										
* 电路板组件：包括印刷电路板及其构成的零部件。										

Environmental Policy

- The product has been designed to enable proper reuse of parts and recycling and should not be thrown away at its end of life.
- Users should contact the local authorized point of collection for recycling and disposing of their end-of-life products.
- Visit the MSI website <https://csr.msi.com/global/pevn_ewaste> and locate a nearby distributor for further recycling information.
- Please visit <<https://us.msi.com/page/recycling>> for information regarding the recycling of your product in the US.

WEEE Statement

European Union: This symbol on the product indicates that this product cannot be discarded as municipal waste. Instead, it is your responsibility to dispose of your waste electrical and electronic equipment by handing it over to a designated collection point for recycling. For more information about where you can drop off your waste equipment for recycling, please contact your local city office, your household waste disposal service or the shop where you purchased the product.



Chemical Substances Information

In compliance with chemical substances regulations, such as the EU REACH Regulation (Regulation EC No. 1907/2006 of the European Parliament and the Council), MSI provides the information of chemical substances in products at:

<https://csr.msi.com/global/index>

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Technical Support

If a problem arises with your product and no solution can be obtained from the user's manual, please contact your place of purchase or local distributor. Alternatively, please visit <https://eps.msi.com/support> for further guidance.



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