

Part Number: WSP-Q40GLR4L

WSP-Q40GLR4L OVERVIEW

The WSP-Q40GLR4L is a transceiver module designed for optical communication applications. The design is compliant to 40GBASE-IR4 of the IEEE P802.3ba standard. The module converts 4 inputs channels of 10 Gbps electrical data to 4 CWDM optical signals, and multiplexes them into a single channel for 40Gbps optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 40 Gbps input into 4 CWDM channels signals, and converts them to electrical data. The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm as members of the CWDM wavelength grid defined in ITU-T G694.2. It contains a duplex LC connector for the optical interface and an 8-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, single-mode fiber (SMF) has to be used. The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.



PRODUCT FEATURES

- LC duplex connector
- 4 CWDM lanes MUX/DEMUX design
- Up to 11.2Gb/s data rate per wavelength
- QSFP+ MSA compliant
- IEEE 802.3ba Electrical Interface
- Digital diagnostic capabilities
- Compliant with QDR/DDR Infiniband data rates
- Up to 100m transmission on OM3 multimode fiber (MM) or 2km transmission on single mode (SM) fiber
- Power Dissipation < 3.5W
- Operating Case Temperature
Standard: 0 to +70

APPLICATIONS

- 40GBASE-LX4 Ethernet Links
- Infiniband QDR and DDR interconnects

FUNCTIONAL DIAGRAM

This product converts the four channel 10 Gbps electrical input data into CWDM optical signals (light), by a driven 4-wavelength Distributed Feedback Laser (DFB) array. The light is combined by the MUX in to 40 Gbps data, propagating out of the transmitter module from the SMF. The receiver module accepts the 40 Gbps CWDM optical signals input, and de-multiplexes it into 4 individual 10Gb/s channels with different wavelengths. Each wavelength is collected by a discrete photo diode, and then output as electric data after being amplified by a TIA. Figure 1 shows the functional block diagram. A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL. Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used. Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP memory map.

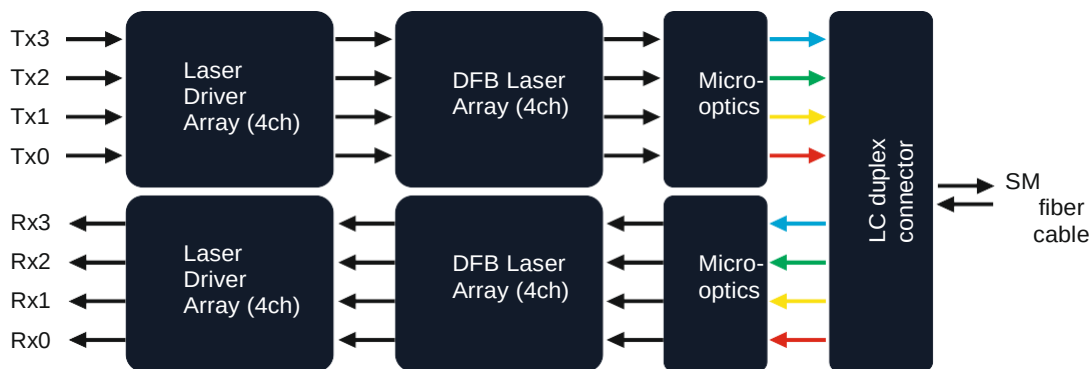


Figure 1. Functional diagram

The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset. Low Power Mode (LPMode) pin is used to set the maximum power consumption for the product in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted. Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a “Low” state. Interrupt (IntL) is an output pin. When Low, it indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_s	-20	+85	degC
Supply Voltage	V_{cc}	0	70	degC
Operating Range		0.002	2	km
Supply Voltage	V_{cc}	3.15	3.47	V

OPTICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Wavelength Assignment	λ_0	1264.5	1271	1277.5	nm
	λ_1	1284.5	1291	1297.5	nm
	λ_2	1304.5	1311	1317.5	nm
	λ_3	1324.5	1331	1337.5	nm

OPTICAL CHARACTERISTICS – TRANSMITTER

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Side-mode Suppression Ratio	$SMSR$	30			dB	
Total Average Launch Power)	P_T			8.3	dBm	
Optical Modulation Amplitude (each Lane)	OMA	-2		+3.5	dBm	
Difference in Launch Power between any two Lanes (OMA)				5	dB	
Extinction Ratio	ER	3.5			dB	
Relative Intensity Noise	RIN			-128	dB/Hz	12dB reflection
-20dB Spectral Width				1	nm	Modulated
Transmitter Reflectance	R_T			-12	dB	
Total Jitter					UI	
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				
Transmitter Output Power Monitoring Accuracy	$OPMA$	-2		2	dB	

Note: Transmitter optical characteristics are measured with a single mode fiber.

OPTICAL CHARACTERISTICS – RECEIVER

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Damage Threshold	THd	3.5			dBm	1
Receiver Sensitivity, each Lane	SR			-11.5	dBm	
Difference in Receive Power between any two Lanes (OMA)				7.5	dB	
Receive Electrical 3 dB upper Cutoff Frequency, each Lane				12.3	GHz	
RSSI Accuracy		-2		2	dB	

Notes:

1. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
2. Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VccI, VccTx, VccRx	-0.5		3.6	V
Data Rate, each Lane			10.3125	11.2	Gbps

ELECTRICAL CHARACTERISTICS TRANSMITTER

Parameter	Symbol	Min	Typ	Max	Unit
Differential Input Impedance		85	100	115	ohm
Differential Input Swing		150		1200	mV
Differential Return Loss		Compliant to IEEE 802.3ba			dB

ELECTRICAL CHARACTERISTICS RECEIVER

Parameter	Symbol	Min	Typ	Max	Unit
Differential Output Impedance		85	100	115	ohm
Differential Output Swing		370		950	mV
Receiver J9 Jitter				0.65	UI
Receiver electrical mask		Compliant to IEEE 802.3ba			

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Output differential return Loss

Compliant to IEEE 802.3ba

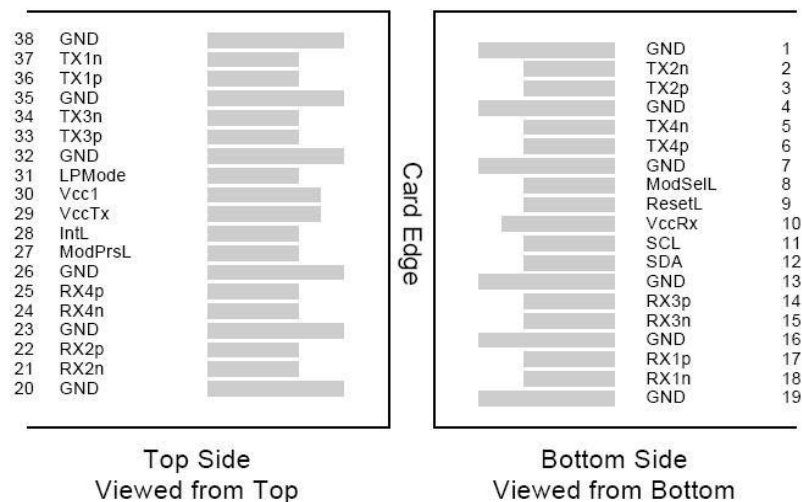
dB

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PIN ASSIGNMENT AND FUNCTION DEFINITIONS

PIN Assignment



PIN Definition

PIN	Signal Name	Description	PIN	Signal Name	Description
1	GND	Ground (1)	20	GND	Ground (1)
2	Tx2n	CML-I Transmitter 2 Inverted Data Input	21	Rx2n	CML-O Receiver 2 Inverted Data Output
3	Tx2p	CML-I Transmitter 2 Non-Inverted Data Input	22	Rx2p	CML-O Receiver 2 Non-Inverted Data Output
4	GND	Ground (1)	23	GND	Ground (1)
5	Tx4n	CML-I Transmitter 4 Inverted Data Input	24	Rx4n	CML-O Receiver 4 Inverted Data Output
6	Tx4p	CML-I Transmitter 4 Non-Inverted Data Input	25	Rx4p	CML-O Receiver 4 Non-Inverted Data Output
7	GND	Ground (1)	26	GND	Ground (1)
8	ModSelL	LVTTLL-I Module Select	27	ModPrsL	Module Present
9	ResetL	LVTTLL-I Module Reset	28	IntL	Interrupt
10	VccRx	+3.3V Power Supply Receiver (2)	29	VccTx	+3.3V Power Supply Transmitter (2)
11	SCL	LVTLL-I/O 2-Wire Serial Interface Clock	30	Vcc1	+3.3V Power Supply
12	SDA	LVTLL-I/O 2-Wire Serial Interface Data	31	LPMODE	LVTTLL-I Low Power Mode
13	GND	Ground (1)	32	GND	Ground (1)
14	Rx3p	CML-O Receiver 3 Non-Inverted Data Output	33	Tx3p	CML-I Transmitter 3 Non-Inverted Data Input
15	Rx3n	CML-O Receiver 3 Inverted Data Output	34	Tx3n	CML-I Transmitter 3 Inverted Data Input
16	GND	Ground (1)	35	GND	Ground (1)
17	Rx1p	CML-O Receiver 1 Non-Inverted Data Output	36	Tx1p	CML-I Transmitter 1 Non-Inverted Data Input
18	Rx1n	CML-O Receiver 1 Inverted Data Output	37	Tx1n	CML-I Transmitter 1 Inverted Data Input
19	GND	Ground (1)	38	GND	Ground (1)

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Notes:

1. All Ground (GND) are common within the QSFP+ module and all module voltages are referenced to this potential unless noted otherwise. Connect these directly to the host board signal common ground plane.
2. V_{ccRx} , V_{cc1} and V_{ccTx} are the receiving and transmission power suppliers and shall be applied concurrently. The connector pins are each rated for a maximum current of 500mA.

MECHANICAL DRAWING

